TWO STAGE INTERCONNECTION NETWORK ARCHITECTURE FOR LINEAR ARRAYS, BINARY TREES, AND CUBES

P.K. Lala, M Tyagi
Department of Electrical Engineering
North Carolina A&T State University
Greensboro, NC 27411

J. Foster
Department of Electrical Engineering
Prairie View A&M University
Prairie View, TX 77446

Abstract: A two stage interconnection network architecture has been proposed. This architecture is reconfigurable into a linear array, binary tree and a cube. To speed up the communication process among the nodes and switches, a 20 bit register has been incorporated in each switch. This architecture makes the interconnection network more flexible and faster in comparison to multistage interconnection networks.

1. Introduction

Interconnection networks are extremely important in parallel and distributed computer systems, and have stimulated much interest in recent years. The interconnection architectures that have been proposed in literature [1], [2], [6], [7], [8], are mostly applicable to one particular type of configuration e.g. linear arrays, binary trees or cube connected nodes. An interconnection network that can accommodate all three of these applications is highly desirable. This network has to have the capability of fully utilizing the interconnected nodes. The interconnection network proposed in this paper can be used to reconfigure the nodes into a linear array, a binary tree or a cube.

2. Interconnection Network Architecture

The proposed interconnection network consists of two stages. Each stage has four switching elements. These switching elements are identified in four rows. Each row has one switch in stage 1 and one in stage 2. Fig. 1 shows the switch interconnections for a sixteen node network. All the switching elements in the network are connected such that access to all nodes is possible. There are two nodes connected to each switching element. To connect these two nodes to the interconnection network, four lines are used in each switch. The line that connects to a node is identified by the node number itself as N1, N2 etc. The lines connecting the two switching stages are identified as Lx where x = 1...4. The switches are identified as Srij, where i = 1 or 2 and j = 1...4. The connections among the switches follow the pattern that the line number of the second stage switch is the same as the row number of the first stage switch i.e. the value Lx for stage 2 is the same as Rx for stage 1.

There are two nodes connected to each switch of stage 1 and stage 2. Thus, a two stage network with four switches per stage can interconnect sixteen nodes. Each node is identified by its node number. Nodes 0 and 8 are connected to SR11, nodes 1 and 9 are connected to SR21, nodes 2 and 10 are connected to SR12, nodes 7 and 15 are connected to SR24. The lines connecting nodes to the switches are bidirectional. As in Ref. [3], the nodes are assumed to have a communication processor to communicate with the switches and other nodes in the
interconnection network. Thus, each node can generate its own control signals. The interconnection network is simplified since there is no need for a central control unit [4].

3. Design of the Switches

The switches in this interconnection network are required to have the capability of reconfiguration into a linear array, a binary tree and a cube. Each switch consists of a control register (CR), transmitting circuit (TC) and the receiving circuit (RC). Transmission Circuit (TC): the circuit helps in transmitting the information from one node to the other node. The nodes must be at different stages i.e. one in stage 1 and the other in stage 2.

Receiver Circuit (RC): The circuit is used for receiving information by stage 1 and stage 2 nodes. Control register (CR): The information stored in CR is used to control the TC and RC circuit connections. It is a 20 bit register with each node in a switch having access to 9 bits of it. Two bits are used to select the mode of computation in a linear array, a binary array or a cube. Each node in a switch requires four bits to load the node address for receiving data from a node. There is an additional bit (T/R) provided to check whether the node is transmitting or receiving. Thus, any node can transmit to or receive data from a node of the other stage. Both nodes in a switch are connected to TC and RC circuits, but only a single operation of either transmitting or receiving data is permitted at a given time.

The four bit address loaded for transmitting and receiving data becomes the control signal for transmitting circuit and receiving circuit i.e. no additional circuitry is required to translate the address into control signals. This cuts down the delay in the reconfiguration of node.

4.1 Configurations for a Linear Array

A linear array has very simple connection topology. It is also referred to as one dimensional mesh. The nodes are arranged in a line and the adjacent nodes are connected. The two end nodes are not connected, and thus have a single link. All the interior nodes have two links. The end nodes are also known as boundary nodes. The boundary nodes have one link that connects them to the internal node. The first node of the linear array is either transmitting to or receiving data from the second node, thus forming only one connection either with transmitting or receiving circuitry. The internal nodes N1 to N6 are connected to both TC and RC circuits since these nodes are receiving as well as transmitting data. Note that the T/R bit allows either transmission of data or receiving it at a given time. This technique minimizes traffic through the interconnection network. The reconfiguration is also simplified as there are few connections to be changed along with the data. It has been assumed for simplicity that the data transmission is from node N0 to N7.

4.2 Configuration for a Binary Tree

The proposed interconnection architecture can be transformed into a binary tree. The binary tree configuration here is proposed in Ref. [5]. The root is formed by node at level 0 to add symmetry to the binary tree architecture. It makes a binary tree with nodes at four levels i.e. level 0, 1, 2 and 3. Node N0 receives data from N1, i.e. the node at level 0 receives data from the node at level 1. N2 and N4 transmit to N1, i.e. N1 receives data from N2 and N4. Node N2 receives data from N3 and N5, N4 receives data from N7 and N15. The nodes at level 3 transmit data to level 2 nodes, they do not receive data. The receiving bit status (in CR) for such nodes is X.
(don't care) as the T/R bit is always set to 1.

The nodes at level 2 receive data from two nodes and then transmit to a single node. In such cases priority is given to the node on the left link. Data is transmitted first by the node on the left link followed by the node on the right link. During this time the T/R bit is set to 0. Once the process of receiving data is complete, the T/R bit is set to 1 and the node address for data transmission is loaded. The bit status is changed by the communication processor of each node.

4.3 Configuration for Cube Connected Nodes

Eight nodes can be connected in cubical order. The nodes are connected such that only a single bit is changed in the address location with reference to the data transferring node on x, y, or z axis. Routing is performed along one axis at a time. For example, a minimal path from the node numbered (a, b, c) to the node numbered (x, y, z) is constructed by moving along the x-axis (x, b, c), then along the y-axis (x, y, c), and finally along the z axis (x, y, z). Thus, any node on the x-axis always has the priority to set up the path and is followed by y and z. Given two nodes A and B, the EX-OR X of the node address for A and B contains a 1 in the coordinates in which the address differs.

5. Conclusion

A two stage interconnection network architecture to interconnect nodes as a linear array, binary tree or a cube has been proposed. This interconnection network and associated switching elements reduce the delay in signal propagation compared to a multistage interconnection network. The ability of this interconnection network to configure into a linear array, binary tree and a cube makes it applicable where multiple configurations are required for computation. The inclusion of a control register in each switch makes each node independent of the central control unit.

REFERENCES

Fig 1. The interconnection network